REDUCED POWER REGISTERED MEMORY MODULE AND METHOD

ABSTRACT OF THE DISCLOSURE

A registered memory module includes a plurality of flip-flops having respective data terminals, respective clock terminals receiving a clock signal and output terminals coupled to a plurality of SDRAM devices in the module. A logic gate decodes respective chip select signals for selecting the SDRAM devices. The logic gate generates an enable signal if a memory access is being directed to any of the SDRAM devices in the module. In one embodiment, the flip-flops include an enable input coupled to receive the enable signal from the logic gate. In another embodiment, the input signals are coupled to the data inputs of the flip-flops through logic gates that are selectively enabled by the enable signal from the logic gate. As a result, the input signals are not latched by transitions of the clock signal when a memory access is not directed to any of the SDRAM devices in the module.